The 2-Channel Serial Audio Interface: A Tutorial

INTRODUCTION

It may come as a surprise to those trying to make their initial investigation into audio systems design that there is a de-facto standard for transferring audio data within a system. Despite the differing naming conventions used within the industry, these apparently different interfaces are essentially identical. For the sake of simplicity, we will use the term Serial Audio Interface (SAI) in this discussion. The Serial Audio Interface is by far the most common mechanism used to transfer two channels of audio data between devices within a system; for instance, from the analog-to-digital converter to the Digital Signal Processor (DSP) and then the digital-to-analog converter, as shown in Figure 1.

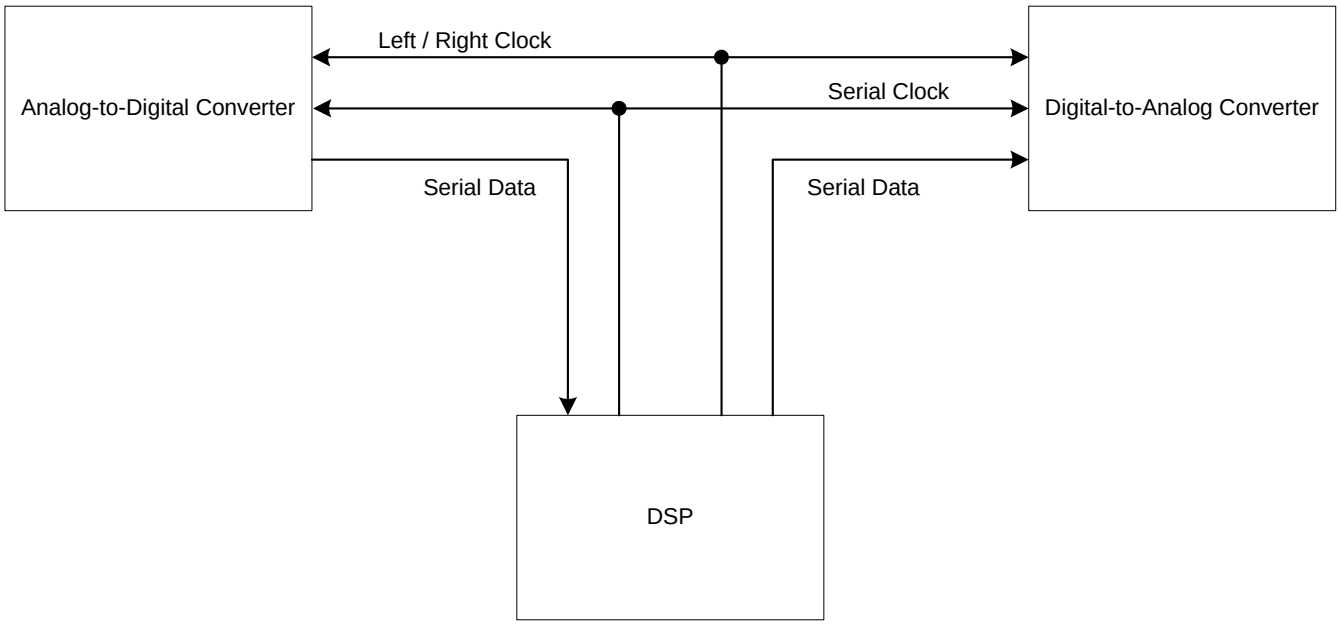

Figure 1 System Block Diagram

1. THE SERIAL AUDIO INTERFACE

The Serial Audio Interface is comprised of two control clocks, the Left / Right and Serial Clocks, and the Serial audio data line. Despite the many different names used for the various clocks, their uses and requirements are nearly identical. A generalized Serial Audio Interface is shown in Figure 2. Some form of this diagram can probably be found in every audio converter and DSP data sheet that has ever been published.

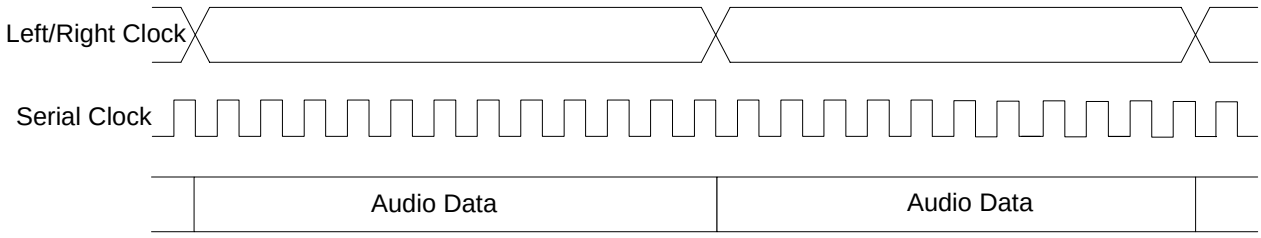

Figure 2 Generic Serial Audio Interface Diagram

1.1 Left/Right Clock

The Left/Right (LRCK) Clock is known by several names, including Word Clock, Frame Clock, Frame Sync, and probably several others. Despite the different names, the use and requirements for this clocking signal are identical. In all applications, the function of this clock signal to identify the audio system sample rate and frame the two channels of audio data that exist on the single audio data line. As a result of the first mentioned function, the required frequency of the Left/Right Clock signal is always at the system audio sample rate, such as 44.1 kHz, 48 kHz, etc. The high and low times of this clock are used to separate or delineate the Left and Right channel data.

1.2 Serial Audio Data

The industry standard for representing Pulse-Coded-Modulation (PCM) audio data is a word comprised of 16 to 32 bits (16- and 24-bit data are the most common) coded in a two's-complement format. The audio data word is always transmitted with the Most Significant Bit (MSB) first. The only common exception to the two's-complement format is when the audio data is represented in one of the many compressed audio formats.

1.3 Serial Clock

The Serial Clock (SCLK) is also often referred to as the Bit Clock. As with the Left/Right Clock, the function is the same regardless of the name. The sole purpose of the Serial Clock is to shift the audio data into or out of the serial audio port. The minimum required frequency for the Serial Clock is directly proportional to the system audio sample rate and the audio word length. Recall that there are two channels of audio data presented in each period of the Left/Right Clock, and the frequency of the Left/Right Clock must be at the audio sample rate. Therefore, the minimum required Serial Clock frequency is twice the audio sample rate times the number of bits in each audio word.

2. THE SERIAL AUDIO INTERFACE FORMATS

There are several de-facto industry standards or formats that define the required alignments and signal polarities between the Left/Right Clock, Serial Clock and the Serial audio data.

2.1 Left-Justified Data Format

The Left-Justified (LJ) format probably got its name from the relationship of the audio data and the Left/Right Clock. Refer to Figure 3 and notice that the MSB of the audio word is coincident with the leading transitions in the Left/Right Clock, or left-justified within the frame. One of the advantages of this format is that it is word-length independent and works properly with audio data words of 16 to 32 bits, assuming there is a sufficient number of serial clocks per Left/Right clock cycle.

Another important aspect of the LJ format is that the audio data for the left channel is presented on the serial data line during the high portion of the Left/Right Clock, and the right channel is presented during the low portion.

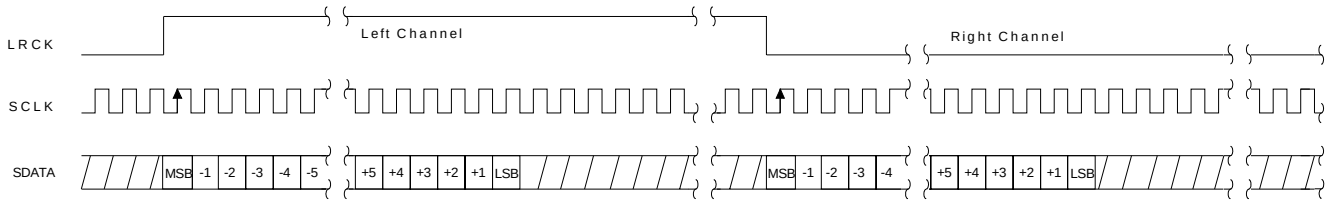

Figure 3 Standard Left-Justified Format

2.2 Right-Justified Data Format

Referring to Figure 4, it is relatively apparent that the Right-Justified (RJ) format is very similar to the Left-Justified format, with the exception of the placement of the audio word within the frame. Notice that the trailing edge of the LSB is coincident with the trailing edge of the Left/Right Clock, or right-justified within the audio frame. The primary disadvantage of this format is that the interface is not word-length independent. As a result, any device that is receiving data in a Right-Justified format must be aware of the transmitted audio word length. This explains why most Digital-to-Analog (D/A) converters are required to support multiple right-justified formats.

As with the Left-Justified format, the audio data for the left channel is presented on the serial data line during the high portion of the Left/Right Clock, and the right channel is presented during the low portion.

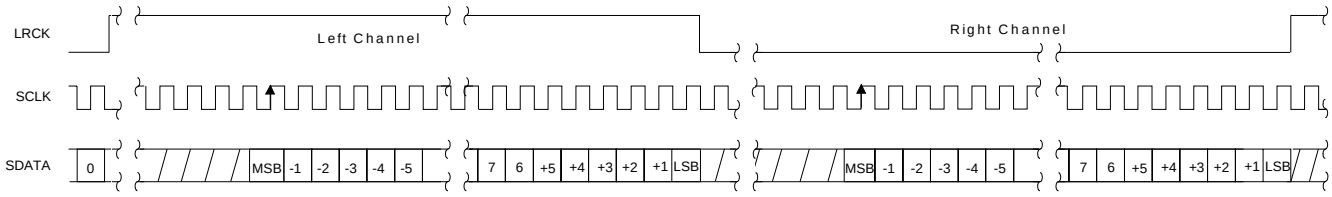

Figure 4 Standard Right-Justified Format

2.3 I²S Data Format

The “Inter-IC Sound” bus (I²S) format was originally developed and standardized by Philips Electronics. The Philips I²S specification can be found at http://www.semiconductors.philips.com/acrobat_download/various/I2SBUS.pdf. Referring to Figure 5, it is relatively apparent that there are significant differences between I²S and the other formats. While I²S retains the word-length independence of the Left-Justified format, notice that the left channel of data is framed by the low time of the Left/Right Clock and the right channel is framed by the high time. Another significant difference is that the MSB of the audio word is shifted or delayed one period of the Serial Clock from the leading edge of the Left/Right Clock.

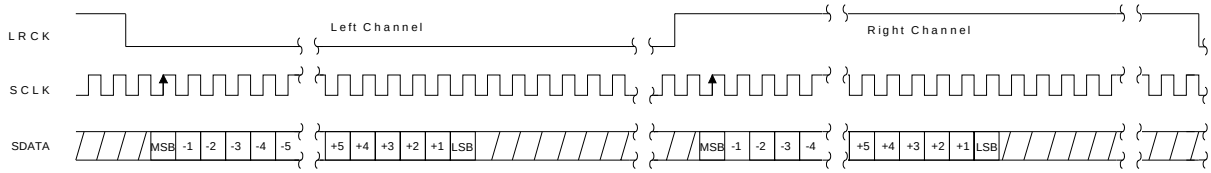

Figure 5 Standard I²S Format

3. TIME ALIGNMENT

A very important aspect of the Serial Audio Interface is the fact that the left/right sample pairs represent simultaneously sampled data or time-aligned data. Another way to look at this relationship is shown in Figure 6, where the same signal is connected to both inputs of an Analog-to-Digital converter. Analyzing the data in left/right sample pairs shows that the left and right channels are time-aligned. However, if the data is analyzed as right/left sample pairs, the signals appear to be time-shifted in relation to each other by ΔT, as shown in Figure 7, where ΔT is equivalent to 1 period of the audio system sample rate.

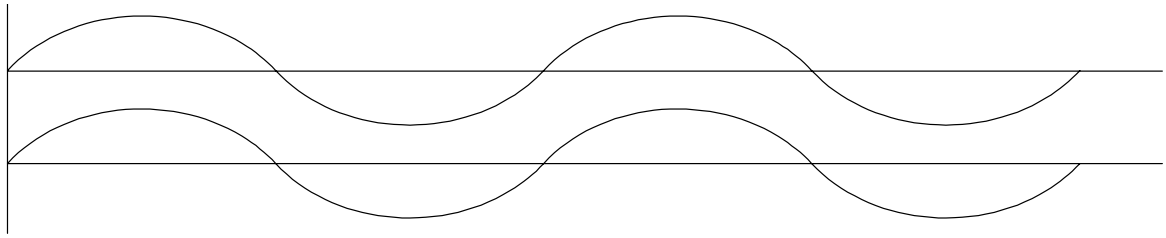

Figure 6 Left/Right Sample Pairs in Time Alignment

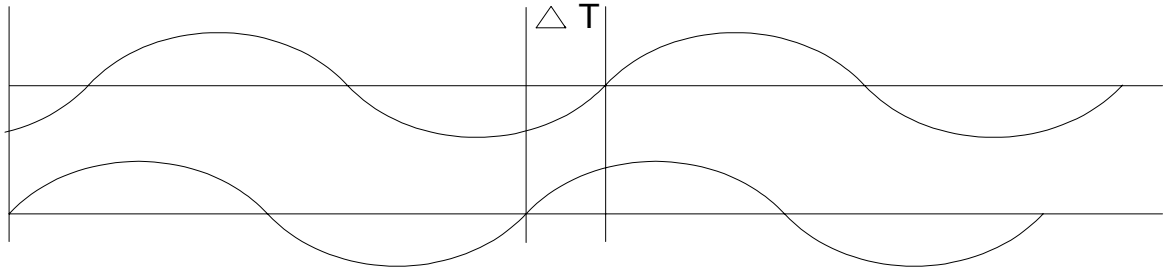

Figure 7 Right/Left Sample Pair in Time Misalignment

4. IMPLEMENTATIONS OF MORE THAN TWO CHANNELS

The Serial Audio Interface can be easily scaled to support larger channel counts simply by adding the appropriate number of serial audio data lines while retaining the single Serial Clock and Left/Right Clock, as shown in Figure 8.

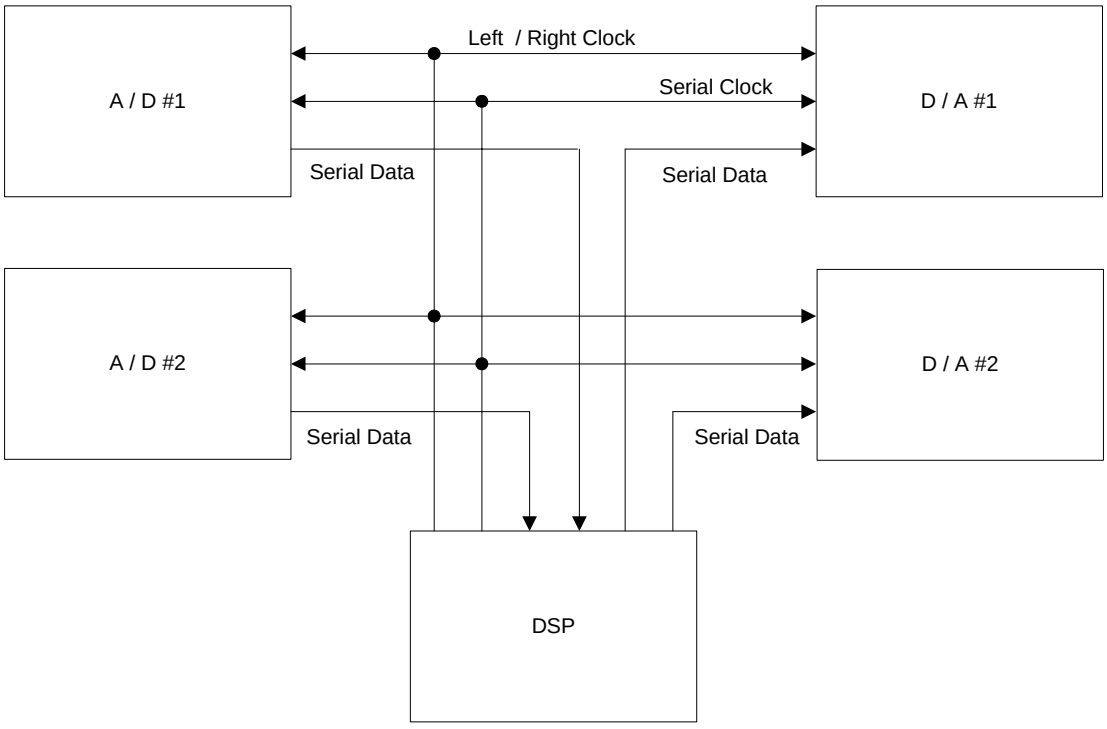

Figure 8 Multi-Channel Serial Audio Interface Diagram

5. REVISION HISTORY

Release	Date	Changes
Revision 1	June 2005	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**